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L-BAND Si POWER V-FET

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ABSTRACT

A new structure Si vertical channel FET —— the covered gate structure has been developed. Compared with the buried gate structure, an increasing power gain by more than 5 dB has been obtained. L-band devices with output power higher than 10W, power gain 6 dB at 1GHz have been fabricated.

The relations between the electrical properties and devices structure parameters are discussed. The excellent temperature performance and other characteristics are reported.

Introduction

Although the J-FET has been reported many years ago[1], it has just been developing repidly after the discovery of the silicon plane technology. From the experimental results reported by S. Teszner et al in 1964[2] and 1972[3], such devices with saturation pentode characteristics have been shown. However, J. Nishizawa et al have worked on the audio high power FET having non-saturation triode characteristics using high resistivity silicon crystal[4].

Why does the frequency performance of V-FET increase slowly for long time? According to the equivalent circuit of the FET, the limited frequency is $f_m = \frac{1}{2 R_g(C_{gs}+C_{gd})}$ where R_g—the gate series resistance, C_{gs}—the gate-source capacitance, C_{gd}—the gate-drain capacitance.

Suppose R_g is quite small the limited frequency can be rewritten as $f'm = \frac{g_m}{2 (C_{gs}+C_{gd})}$, where g_m is the transconductance of device, $g_m = \frac{g'_m}{1+r_s g'_m}$, g'_m is the intrinsic transconductance, r_s is the source series resistance.

Thus it can be seen, in order to obtain excellent frequency performance, the parameters R_g, r_s, and C_{gd} should be as small as possible, the transconductance of the device should be as high as possible. For the conventional V-FET it has been limited to further reduce their value. That is just the reason why the frequency properties of V-FET increased so slowly.

In recent years J. Nishizawa et al[5] have made the SIT (Static Induction Transistor) with ordinary plane technology. The parameters R_g, C_{gs} and r_s of such devices have been reduced. Thus the frequency performance of the device has been improved, but the process is complex.

We have developed a new structure V-FET — the covered gate structure. It maintains the advantages of the ordinary buried gate structure, such as the simple technology and larger transconductance of the unit gate width. And, further more, the obviously decreased values of R_g and C_{gs} shows that the improvement of the frequency performance of device.

Device Structure Analysis

N^+ type single crystal silicon with lower resistivity is used as substrate. The n type epitaxial layer 8-15 with the carrier concentration $n = 1-5\times10^{14}$ cm^{-3} is grown by VPE. The p^+ type gate region is formed by diffusion of boron. The diffusion depth must be controlled carefully according to the design. The gates are covered with a dielectric layer. The source region is formed with low temperature epitaxy. Fig. 1 shows the different gate-source capacitance C_{gs} of the covered gate FET and the ordinary buried gate FET. We can see that the capacitance C_{gs} is greatly reduced in the covered gate structure.

Moreover, in the covered gate structure the self-doping which often occurs in the ordinary buried gate structure can be avoided for heavy doping of the gate region. Thus in the covered gate structure the gate series resistance r_g would be very small. This is impossible for the ordinary buried gate structure. The covered gate

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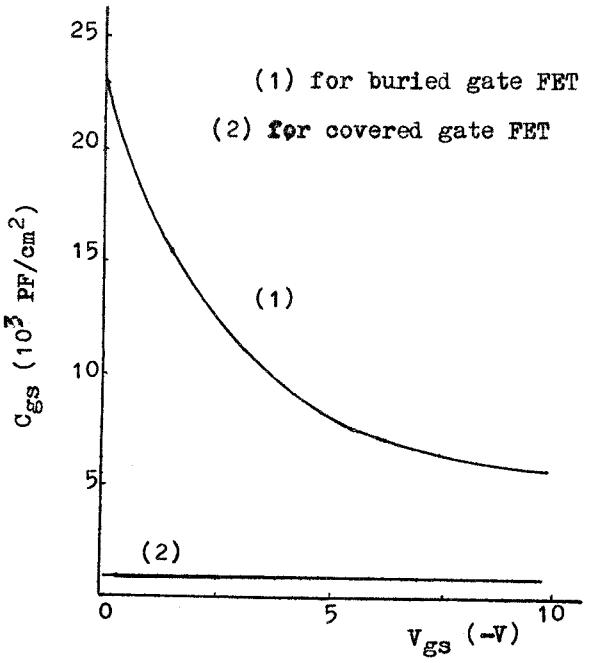

Fig.1 The dependence of C_{gs} on V_{gs} for the covered gate and buried gate V-FET

structure obviously reduces C_{gs} and r_g. Thus it greatly improves operating frequency and power gain of the device.

We have discussed the principle of operation about such device. Assuming the source series resistance R_s to be zero, the equation of the source-drain current can be written as:

$$I_{ds} = \frac{V_p + DV_{GD} - V_{gs}}{R_{co} - AV_{GD}^{1/2}} \qquad \text{---------(1)}$$

where V_p is the pinch-off voltage, D—the osmotic coefficient, R_{co}—the channel equivallent resistance when $V_{gs} = 0$ and $V_{GD} = V_p$. A is constant which depends on the structure parameters.

Such device has non-saturation triode characteristic.

"D" and " V_p " can be measured with following method. A variable voltage V_{gd} is applied to the gate-drain, then the gate-source potential V_{gs} is measured. The results are shown in Fig. 2. The voltage corresponding to the turning point "P" is the pinch-off voltage "V_p". The slope of the line "PF" is the osmotic coefficient "D". The gate-source C_{gs} can be expressed as following:

$$C_{gs} = \varepsilon \varepsilon_o / d_o \qquad \text{----------(2)}$$

where ε is the dielectric constant of the di-

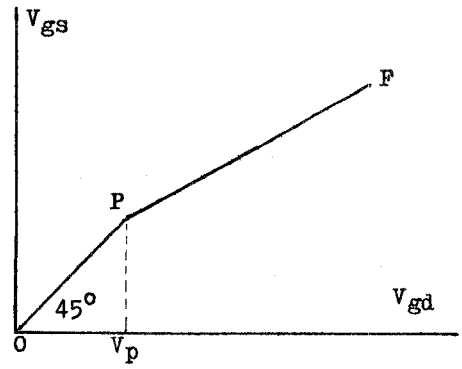

Fig.2 The dependence of V_{gs} on V_{gd} for new structure V-FET

electric layer, ε_o is the vacuum dielectric constant, d_o is the thickness of the dielectric layer.

According the equivalent circuit the maximum power gain can be expressed as following:

$$G_{mA} = \frac{g_m^2}{4W^2 C_{gs}^2 (r_s + r_g)\ W^2 C_{gd}^2 r_D + g_{ds}} \qquad \text{----(3)}$$

where g_m is the transconductance, g_{ds} is the source-drain conductance, r_s, r_g, r_d are the source, gate and drain series resistance respectively.

Device Performance

L-band devices with output power higher than 10W, gain more than 6 dB at 1GHz have been fabricated using the covered gate structure.

Such devices have following outstanding advantages compared with the silicon power bipolar

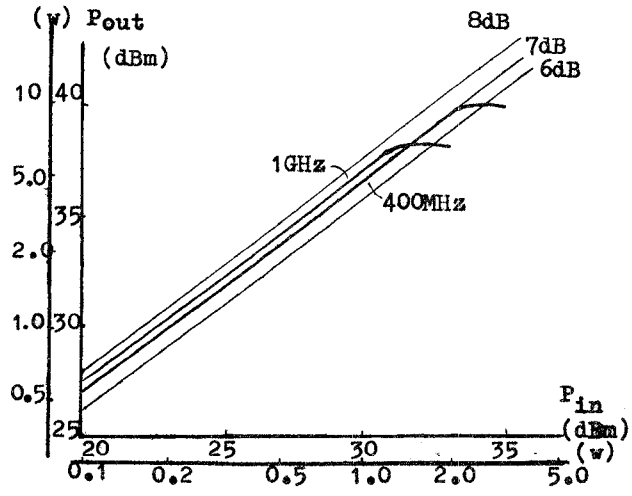

Fig. 3 Output power P_{out} vs input power P_{in}

transistor.

(a) A large linear operating area. Fig. 3 shows the amplification characteristics of two typical covered gate devices. The output power of the 1 dB gain compression point amounts to 80 percent of the maximum output power. For 0.5 dB gain compression point—70 percent. These properties can not be obtained for the bipolar transistor.

(b) Excellent temperature performance. Such device is one of the majority carrier devices. It has excellent temperature performance.

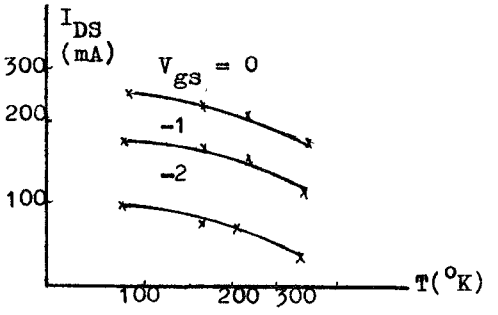

Fig.4 The dependence of I_{DS} on temperature

Fig. 4 shows the source-drain current I_{DS} as a function of the temperature for different source- gate voltages. Fig. 5 shows the transconductance as a function of the temperature. In order to compare, the current amplification coeficient β of the bipolar transistor 3DF1B, as a function of the temperature also is given in Fig. 5. From -196°C to 125°C the transconductance g_m reduced by 60 %, but β varied about 16 times.

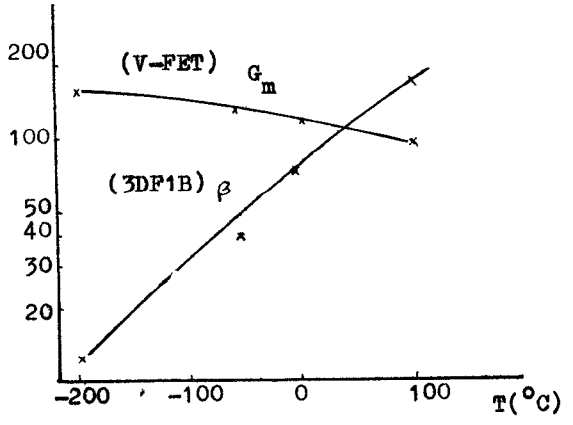

Fig. 5 G_m and β as a function of temperature

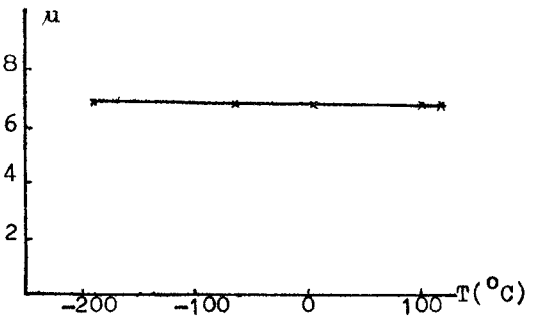

Fig.6 μ vs temperature

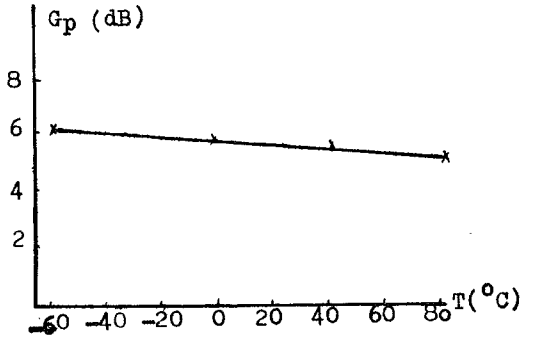

Fig.7 Power gain G_p vs temperature

Fig. 6 and Fig. 7 show the voltage amplification ratio μ and the power gain G_p as a function of temperature respectively.

They are nearly no change over the whole temperature range. Further more, the covered gate FET has also no second breakdown as well as the good radiation-resistance.

Acknowledgment

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Reference

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